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WHAT IS CLAIMED IS:

1. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising:

a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value;

a second candidate output value producing unit connected for receiving said input value and operable, during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

an in-range value determining unit which determines which one of said first and second candidate output values is within said preselected output-value range; and

an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

2. Mapping circuitry as claimed in claim 1, wherein said in-range value determining unit is operable to determine which one of said first and second candidate

output values is within said preselected output-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.

3. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising:

a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value;

a second candidate output value producing unit connected for receiving said input value and operable to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

an in-range value determining unit operable to determine, during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and

an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined

to be within said output-value range.

4. Mapping circuitry as claimed in claim 1 or 3, further comprising:

an input range determining unit connected for receiving said input value and operable to determine whether said input value is within said preselected input-value range; and

a third candidate output value producing unit which produces a third candidate output value;

wherein said output value selection unit is operable, when said input range determining unit determines that said input value is outside said preselected input-value range, to select as said corresponding output value said third candidate output value.

5. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is connected for receiving said input value and said third candidate output value is dependent upon said input value.

6. Mapping circuitry as claimed in claim 5, wherein said third candidate output value is equal to said input value.

7. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.

8. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is operable to produce said third candidate output value during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.

9. Mapping circuitry as claimed in claim 1 or 3, wherein at least one of said output-range limit values is variable during operation of the circuitry.

10. Mapping circuitry as claimed in claim 1 or 3, wherein the span of the preselected output-value range is greater than the span of the preselected input-value range.

11. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range by producing a detection value that differs by a third offset value from the received input value, and detecting when a predetermined bit of the detection value has a predetermined logic value.

12. Mapping circuitry as claimed in claim 11, wherein said third offset value is set in dependence upon an input-range limit value defining one of the limits of the predetermined input-value range.

13. Mapping circuitry as claimed in claim 12, wherein the detection value is produced by adding the third offset value to the received input value.

14. Mapping circuitry as claimed in claim 11, wherein said predetermined bit is the most significant bit of the produced detection value.

15. Mapping circuitry as claimed in claim 1 or 3, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining said difference between them.

16. Mapping circuitry as claimed in claim 1 or 3, wherein said in-range value determining unit is operable to produce a detection value that differs by an in-range offset value from the received input value, and to determine that the in-range output value is the first candidate output value when a preselected bit of

the produced detection value has a first logic value and that the in-range candidate output value as the second candidate output value when that bit has a second logic value.

17. Mapping circuitry as claimed in claim 16, wherein said in-range offset value differs from the first offset value by one of said output-range limit values and differs from the second offset value by the other of said output-range limit values.

18. Mapping circuitry as claimed in claim 16, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining said difference between them, and wherein said offset varying unit also varies said in-range offset value when said first and second offset values are varied so as to leave unchanged the respective differences between the first and in-range offset values and between the second and in-range offset values.

19. Mapping circuitry as claimed in claim 16, wherein the in-range offset value is dependent upon an input-range limit value defining one of the limits of the preselected input-value range.

20. Mapping circuitry as claimed in claim 18, wherein the detection value is produced by adding the in-range offset value to the received input value.

21. Mapping circuitry as claimed in claim 16, wherein said preselected bit is the most significant bit of the produced detection value.

22. A processor comprising:

an instruction issuing unit which issues instructions;

at least one instruction executing unit which executes the issued instructions;

a register file, having a plurality of physical registers; and

mapping circuitry which maps an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said input value being a logical register identifier specified by one of said instructions, and said output value being a physical register identifier used for identifying one of the physical registers within said register file that corresponds to the specified logical register identifier;

wherein said mapping circuitry comprises:

a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value;

a second candidate output value producing unit connected for receiving said input value and operable, during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

an in-range value determining unit which determines which one of said first and second candidate output values is within said preselected

output-value range; and

an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

23. A processor comprising:

an instruction issuing unit which issues instructions;

at least one instruction executing unit which executes the issued instructions;

a register file, having a plurality of physical registers; and

mapping circuitry which maps an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said input value being a logical register identifier specified by one of said instructions, and said output value being a physical register identifier used for identifying one of the physical registers within said register file that corresponds to the specified logical register identifier;

wherein said mapping circuitry comprises:

a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value;

a second candidate output value producing unit connected for receiving said input value and operable to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective

output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

an in-range value determining unit operable to determine, during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and

an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

24. A processor as claimed in claim 22 or 23, wherein said register file comprises a dynamically-named region and mapping-circuitry output values within the predetermined output-value range provide said physical register identifiers of those physical registers within said dynamically-named region.

25. A processor as claimed in claim 22 or 23, wherein said register file comprises a statically-named region and mapping-circuitry output values outside the predetermined output-value range provide said physical register identifiers of those physical registers within said statically-named region.

26. A mapping method for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said method comprising:

producing a first candidate output value that differs by a first offset value from the received input value;

producing, during production of said first candidate output value, a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

determining which one of said first and second candidate output values is within said preselected output-value range; and

selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

27. A mapping method for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said method comprising:

producing a first candidate output value that differs by a first offset value from the received input value;

producing a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value

range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

determining, during production of one or both of said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and

selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

28. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising:

first candidate output value producing means connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value;

second candidate output value producing means connected for receiving said input value and operable, during operation of said first candidate output value producing means to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those

two values is outside that range;

in-range value determining means for determining which one of said first and second candidate output values is within said preselected output-value range; and

output value selection means for selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

29. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising:

first candidate output value producing means connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value;

second candidate output value producing means connected for receiving said input value and operable to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range;

in-range value determining means operable to determine, during operation of one or both of said first and second candidate value producing means to produce said first and second candidate output values, which one of said first and second candidate output

values is within said preselected output-value range; and

output value selection means for selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.